TITLE **Compromise proposal for SDSL Testloops**

PROJECT SDSL

SOURCE: KPN
Author: Rob van den Brink, KPN Research

CONTACT R.F.M. van den Brink
KPN Research,
PO Box 421
2260 AK Leidschendam
The Netherlands
tel: +31 70 3325389
fax: +31 70 3326477
email: R.F.M.vandenBrink@research.kpn.com

STATUS For decision

ABSTRACT This proposal is a compromise between the various proposals, and is based on updating the existing HDSL testloops. By changing the way they are specified many of the KPN objections against the existing HDSL loops can be removed. The issue of extending the frequency range beyond ADSL frequencies is still inadequately solved.

1. Problem description

The objective of transmission conformance test for xDSL modems is to prove that they function well under realistic conditions. The testloops in these tests shall therefore cover the insertion losses, group delays and impedance mismatches that can be observed in a wide range op operational access networks.

The ETSI-TM6 proposals so far on SDSL testloops can be subdivided into two groups [1]:
1. proposals based on the old HDSL testloops [2,3,4]
2. proposals based on the new VDSL testloops [5,6] (plus additional loops with bridge-taps [7])

The various objectives behind these proposals are quite different. The most striking ones are:
- (1) Define loops that reuse existing HDSL test equipment. This enables a comparison in performance between SDSL and HDSL.
- (2) Define one set of loops that can cover all long-range xDSL systems, including ADSL (this requires a specification up to, say 2MHz)
- (2) Define loops that cover the full impedance range from 100Ω to 150Ω, because this is the range of *commonly* used distribution cables.
- (2) Keep the number of loops as small as possible

It is in nobody's interest to delay the progress on SDSL by a long testloop discussion. That's why this proposal is a compromise between the HDSL- and VDSL-based proposals. This compromise is based on updating the existing HDSL testloops, but changes the way they are specified. KPN Research is still not comfortable with this solution, because of
- the unneccesary complexity of these HDSL loops (see figure 1), and
- the lack of reliable cable measurements that should justify the specification of the cable sections.

That's why VDSL has provided a much better basis for testloops, but KPN can accept an HDSL-based compromise, simply because HDSL-based loops appeared to have quite a lot of supporters.

1.1. How are the main objections solved?

The main objections from KPN against the existing HDSL loops can be solved by changing the way the SDSL loops are specified. This should have no impact on the loop characteristics

itselves, but enables an ***unambiguous specification*** that can also address several issues that are ***typical for SDSL and ADSL***. This modified specification in this proposal enables:

- Extension of the *frequency range* of the specification, to enable their use for other xDSL technologies such as ADSL. The use of two-port cable models, in stead of RLCG tables at a few fixed frequencies, can extend the HDSL specification from 500kHz up to 2 MHz and beyond.
- Unambiguous scaling of looplength, for various bitrates, over a much wider range than is required for HDSL. The use of cable models is essential here to prevent ambiguity caused by interpolating the frequency dependent RLCG parameters.
- The application of the SDSL noise model, because that noise is looplength dependent. An unabiguous specification what the length of each loop is, is crucial here.

Our objectives are: as close as possible to existing HDSL loops and commonly used cable simulators.

1.2. Issues that must be solved, before acceptance

The weakest point of updating HDSL testloops is **the lack of reliable data** above 500kHz.

- The only models that are made available are the cable models that are suggested in TD10 [3]. They are not based on real cables, but fitted to the old HDSL loops (specified up to 500kHz). It is unclear how realistic their extrapolation is from 500kHz to 2MHz, and some of them do not fully match the *current* HDSL specifications. These models are therefore not perfect, but KPN has never seen other ones.
- Using ETSI ADSL RLCG-tables cannot solve this issue because ADSL testloops are based on totally different cables, that were given –unfortunately- the same name as the sections in the HDSL testloops. This illustrated why adequate information for a **full two-port model** is still lacking.

KPN can only accept this compromise if cable simulators can be build, or real cables can be made available, that meet these testloop requirements, at a specified precision (see section 2.4). In addition, the loop specification must not exclude a test application for ADSL (*so specified beyond the highest ADSL frequencies, say up to 2MHz).*

At least one of the following pragmatic solutions can solve this problem.

- A full two-port characterization, up to 2MHz, will be performed on commercially available, and commonly used, cable simulators that suits the HDSL needs. The cable model that will be extracted from these measurements will serve as specification of the individual cable sections.
- A full two-port characterization, up to 2MHz, will be performed on the cables that formed the basis for the HDSL testloops. The cable model that will be extracted from these measurements will serve as specification of the individual cable sections.

If this issue cannot be solved, there is no other alternative for defining testloops, than using models from existing cables as brought together in [10]. In that case, the VDSL testloops (plus additional bridge-tapped loop [7]) are favourable.

1.3. Basic proposal

The text in the next chapter is intended to be literal text, for inclusion into the SDSL draft. The phrase “Annex A” refers to an annex on cable models, as included in [6].
Figure 2 and 3 are based on HDSL testloops (up to 500kHz), and beyond that frequency based on an “educated guess” from KPN. The primary parameters that resulted from this guess are shown in section 4. Note that we considered one of the “PE08” specs at 500kHz in the HDSL standard as implausible, so it has been overruled by our “educated guess” (bold in section 4).

The purpose of this guess was to produce figure 2 and 3, because such an approach is quite tricky. Its possible that this guess violates physical laws, so that no-one can ever build a cable simulator that meets these parameters. That’s why the literal text proposal for the SDSL draft refers to cable models in annex A, while their description is left empty and for further study. Consultronics made in [4] a similar “educated guess” for the characteristic impedance up to 1 MHz. Their guess is not in contradiction with the one we used in the section 4 and in figure 2 and 3.

2. Test loops

The purpose of the test loops shown in Figure 1 is to stress xDSL transceivers under a wide range of different conditions that can be expected when deploying xDSL in real access networks

2.1. Functional description

The test loops in figure 1 are an artificial mixture of cable sections. A number of different loops has been used to represent a wide range of cable impedances, and to represent ripple in amplitude and phase characteristics of the testloop transfer function.

- The length of the individual loops are such chosen that the transmission characteristics of all loops are comparable (see figure 2). This has been achieved by normalizing the *electrical* length of the loops (insertion loss at a well chosen test frequency). The purpose of this is to stress the equalizer of the xDSL modem under test similarly over all loops, when testing xDSL at a specific bitrate. The total length of each loop is described in terms of *physical* length, and the length of the individual sections as a fixed fraction of this total. If implementation tolerances of one testloop causes that its resulting *electrical* length is out of specification, then its total physical length shall be scaled accordingly to correct this error.
- The impedance characteristics of these loops are such chosen that they cover the impedances of a wide range of distribution cables that are commonly used in Europe (see Figure 3). The purpose of a wide range of impedances is to stress the echo cancelation of the xDSL modem under test. This effect has been emphasized by implementing some loops with highly mismatched cable sections.
- One test loop includes bridged taps to achieve rapid variations in amplitude and phase characteristics of the cable transfer function. In some European access networks, these bridge taps have been implemented in the past, which stresses the xDSL modem under test differently.
- Loop #1 is a symbolic name for a loop with zero (or near zero) length, to prove that the xDSL transceiver under test can handle the potentially high signal levels when two transceivers are directly interconnected.

> **ED NOTE** It is posible that the approach of "normalizing" the electrical length can be improved by a more sophisticated approach (e.g. equivalent loss, impulse response). In that case, the length of each loop remains specified in terms of electrical length (at a well chosen center frequency) but each loop has a (slightly) different electrical length. Such an improvement has only impact to the numbers in table 1 and 2, and not on the topology description in figure 1. The numbers in table 1 and 2 are for further study.

2.2. Testloop topology

The topology of the loops is specified in figure 1. The transfer function of all the loops for each payload bit-rate is shown in Figure 2. The variation of input impedance for the various test loops is shown in Figure 3. The two-port cable models that are used to describe the individual sections of the loops are specified in Annex A.

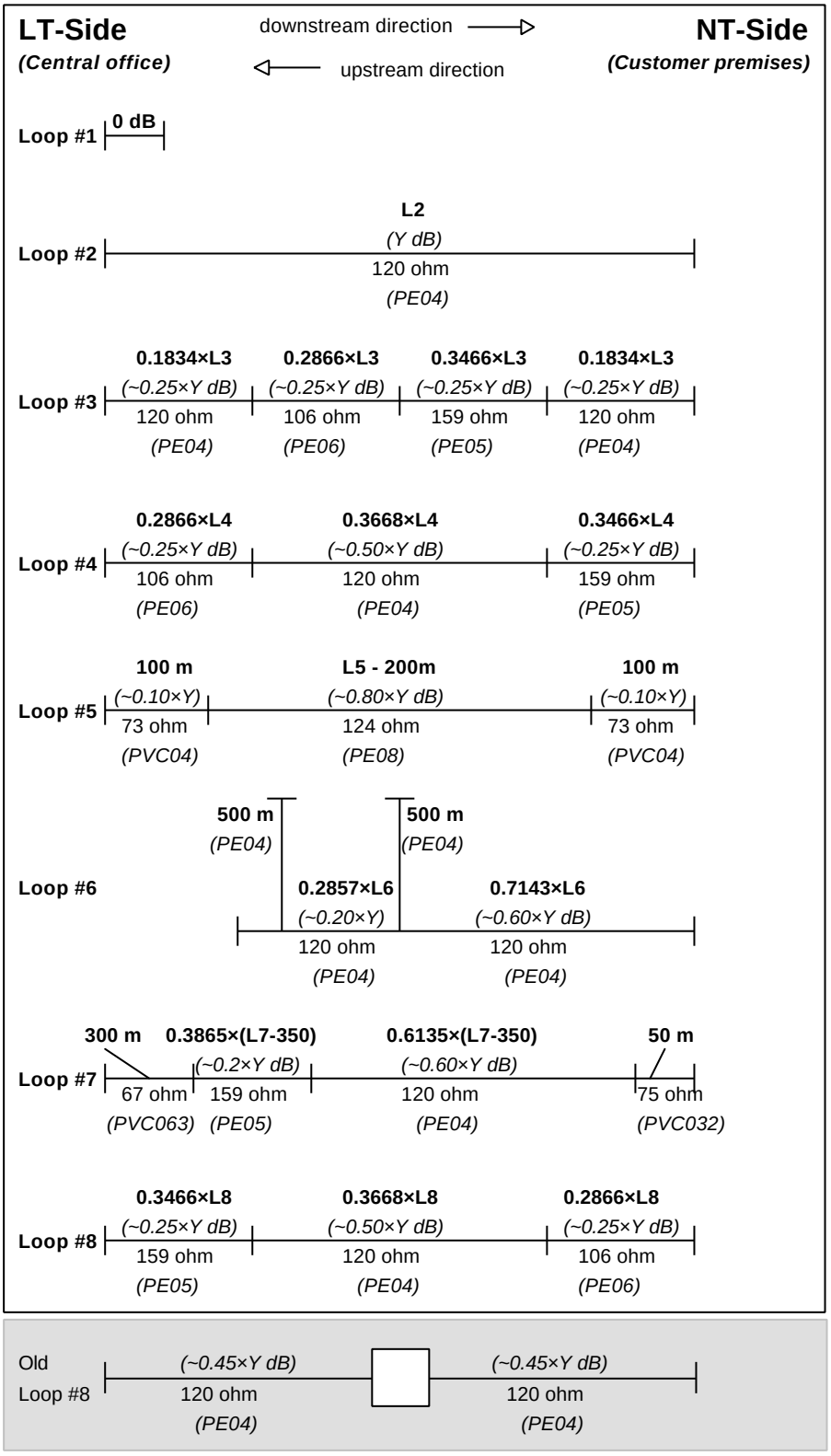

Figure 1: Test loop topology, that is made as similar as possible to existing HDSL test loops. Mark that loop#8 is the same as loop #4, but reversed in transmission direction. The physical lengths L1 to L8 are specified in table 1. The symbolic labels (e.g. "PE04") refer to the two-port cable models that are specified in Annex A. The impedances refer to the characteristic impedance of each section, at 300 kHz, and is for information only. The same applies to the "Y"-values, that refer to what portion of the characteristic insertion loss is accounted for each section.

ED NOTE The ***old*** HDSL Loop #8 is the same as HDSL loop #2, but with an additional insertion network for common mode rejection tests. This is not a testloop issue but an EMC issue. Recently, common mode rejection tests are described in great detail in IEC-DIS1000-4-6 [11], and requires injection at the ***end*** of the testloops, closer than 30cm from the xDSL modem under test. That's why the old "loop" #8 has been grayed-out here, to demonstrate this removal.

ED NOTE The "***new***" Loop #8 is the same as loop #4, but with reversed transmission direction. This is to include loops that can stress downstream performance with high impedance cables (>150 ohm). Loop #8 is required to solved this.

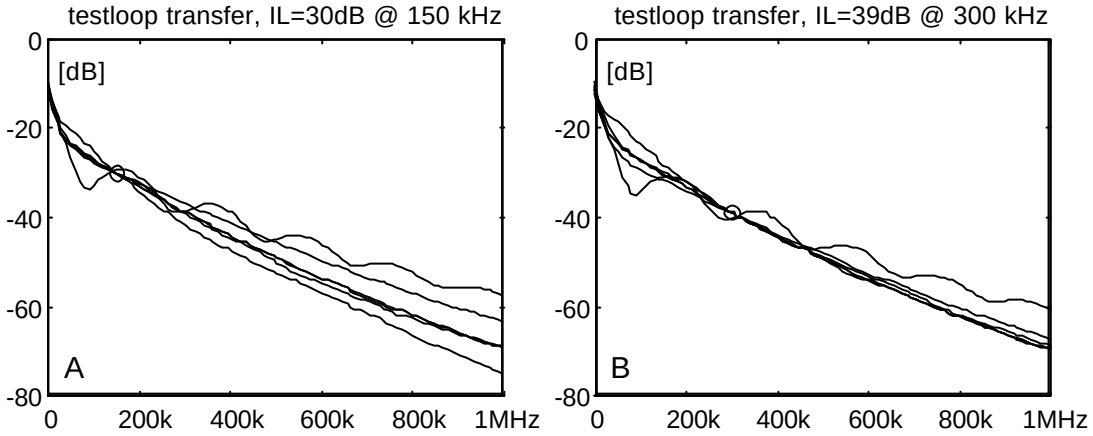

Figure 2: Examples of calculated transfer functions (into 135W) of test-loop #2 to #8. In figure 2a the electrical length of each loop is normalized at 150 kHz (30 dB loss in this example), and in figure 2b at 300 kHz (39 dB in this example). The choise for this test frequency is closely related to the PSD of the xDSL modem under test, and this PSD may vary with the payload bitrate.

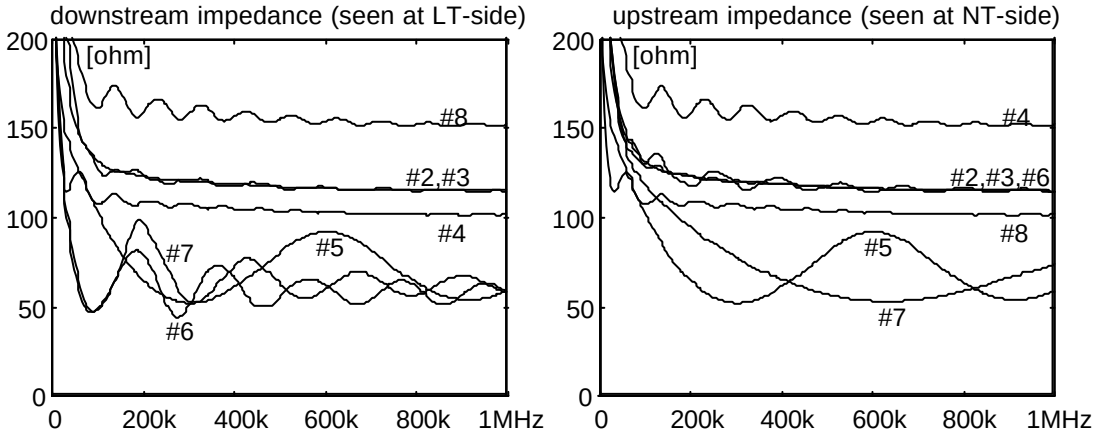

Figure 3: Calculated variation of input impedance (absolute value) of testloop #2 to #8. When the cable is relatively long, these impedances become more or less length independent.

ED NOTE This plot demonstrates why the new loop #8 (as the reversal of loop #4) is required. If it was absent, the downstream echo cancellation of SDSL could not be stressed with high impedances (>150 Ω)

2.3. Testloop length

The length of each test loop for SDSL modems is specified in table 1. The specified insertion loss at the specified test frequency and 135Ω impedance (*electrical* length) is mandatory. If implementation tolerances of one testloop causes that its resulting *electrical* length is out of specification, then its total *physical* length shall be scaled accordingly to adjust this error.

The test frequency is chosen to be a typical mid-band frequency in the spectrum of long range xDSL systems. The length is chosen to be a typical maximum value that can be handled correctly by the xDSL transceiver under test. This value is bitrate dependent; the higher the payload bit-rate, the lower the insertion loss is that can be handled in practice.

Payload Bitrate [kb/s]	f_T [kHz]	IL_0 [dB] @f_T, @135 W	L1 [m]	L2 [m]	L3 [m]	L4 [m]	L5 [m]	L6 [m] =0.8×L2	L7 [m]	L8 [m] = L4
384	150	**47**.13	< 3	4500	6096.0	6104.0	12218.0	3600.0	5175.0	6104.0
512	150	**43**.56	< 3	4160	5635.0	5641.0	11221.0	3328.0	4767.0	5641.0
768	150	**38**.33	< 3	3662	4960.7	4962.0	9759.7	2929.6	4154.7	4962.0
1024	150	**34**.77	< 3	3323	4496.5	4501.8	8765.7	2658.4	3728.0	4501.8
1280	150	**32**.94	< 3	3148	4256.8	4264.1	8251.9	2518.4	3510.4	4264.1
1536	150	**29**.03	< 3	2776	3750.4	3755.0	7161.2	2220.8	3065.3	3755.0
2048	150	**25**.09	< 3	2400	3229.1	3235.2	6059.0	1920.0	2626.1	3235.2
2304	150	**23**.75	< 3	2273	3055.3	3061.8	5683.9	1818.4	2475.6	3061.8

Table 1: Approximation for the physical length of the SDSL testloops, calculated for different electrical lengths.

ED NOTE The numbers here are an example only. The insertion loss values at 150 kHz were taken from TD8 and TD10 [2.3] (Edinburgh). When the PSD for SDSL has been defined, it is plausible that these values may change. The same applies for the 150 kHz test frequencies. The PSD may give reason to make this bitrate dependent if it suits better to the chosen PSD. This topic is for further study.

Realistic electrical length values shall be based on the results of performance simulations that show what realistic values are.

Payload Bitrate [kb/s]	f_T [kHz]	IL_0 [dB] @f_T, @135 W	L1 [m]	L2 [m]	L3 [m]	L4 [m]	L5 [m]	L6 [m] =0.8×L2	L7 [m]	L8 [m] = L4

Table 2: Approximation for the physical length of the ADSL testloops, calculated for different electrical lengths.

ED NOTE This table is intended for future adoption of these test loops for ADSL. The topology of these new ADSL loops are intended to be the same as for SDSL. The length of these new ADSL testloops are for further study

2.4. Testloop accuracy

The different cable sections in the topology of Figure 1 are specified by two-port cable models that serve as a template for real twisted-pair cables. Cable simulators as well as real cables can be used for these test loops. The associated models and line constants are specified in Annex A.
The characteristics of each testloop, with cascaded sections, shall approximate the models within a specified accuracy. This accuracy specification does not hold for the individual sections.

- The magnitude of the test-loop insertion loss shall approximate the insertion loss of the specified models within 3% on a dB scale, between $0{,}1\times f_T$ and $6\times f_T$.
- The magnitude of the test-loop characteristic impedance shall approximate the characteristic impedance of the specified models within 7% on a linear scale, between $0{,}1\times f_T$ and $6\times f_T$
- The group delay of the test-loop shall approximate the group delay of the specified cascaded models within 3% on a linear scale, between $0{,}1\times f_T$ and $6\times f_T$.

Annex A: Line constants for the test loops

This appendix details the typical line constants for the cable sections in the testloops. The primary cable parameters vary with the frequency. Their typical values may be calculated at any frequency (up to xx MHz) by using empirical models. The formulas in Table A.1 define the formal model, and the line constants in Table A.2 and Table A.3 the associated parameters.
They may be used to calculate the primary parameters $\{Z_s,\ Y_p\}$ of the cable sections, per unit length.

NOTE: Conductance becomes significant at high frequencies and must not be ignored.

<FOR FURTHER STUDY>	[Ω/km] [S/km]

Table A.1 : The formal models, that may be used to calculate the cable parameters in the test loops, in combination with the line constants given in Table A.2

symbolic name							
“PE04” **“PE05”** **“PE06”** **“PE08”** **“PVC032”** **“PVC04”** **“PVC063”**		<FOR	FURTHER	STUDY>			

Table A.2 : Line constants for the cable sections in the test loops.

Insertion loss and return loss of a cable section can be calculated from the primary parameters $\{Z_s,\ Y_p\}$ per unit length (L_0) by evaluating the two-port s-parameters, normalized to $\mathbf{R_v} = 135\ \Omega$.

$Z_{sx} = (L/L_0)\cdot Z_s$ $Y_{sx} = (L/L_0)\cdot Y_s$	$\gamma_x = \sqrt{Z_{sx}\cdot Y_{px}}$ $Z_0 = \sqrt{Z_{sx}/Y_{px}}$	$\alpha_x = real(\gamma_x)$ $\beta_x = imag(\gamma_x)$	$R_{sx} = real(Z_{sx})$ $L_{sx} = imag(Z_{sx}/\omega)$	$G_{px} = real(Y_{px})$ $C_{px} = imag(Y_{px}/\omega)$

$$\mathbf{S} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} = \frac{1}{(Z_0/R_v + R_v/Z_0)\cdot\tanh(\gamma_x)+2} \times \begin{bmatrix} (Z_0/R_v - R_v/Z_0)\cdot\tanh(\gamma_x) & 2/\cosh(\gamma_x) \\ 2/\cosh(\gamma_x) & (Z_0/R_v - R_v/Z_0)\cdot\tanh(\gamma_x) \end{bmatrix}$$

insertion loss: $1/s_{21}$
return loss: $1/s_{11}$

The s-parameters of two cable sections (a and b) in cascade can be calculated from the s-parameters $\mathbf{S}_a$ and $\mathbf{S}_b$ as described below:

$$\mathbf{S} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix} = \frac{1}{1-s_{22a}\cdot s_{11b}} \cdot \begin{bmatrix} s_{11a}-\Delta_{sa}\cdot s_{11b} & s_{12b}\cdot s_{12a} \\ s_{21a}\cdot s_{21b} & s_{22b}-\Delta_{sb}\cdot s_{22a} \end{bmatrix} \qquad \Delta_s = s_{11}\cdot s_{22} - s_{12}\cdot s_{21}$$

3. References

[1] Rob van den Brink, KPN, *"Results of the ad hoc group on SDSL test loops*", ETSI-TM6 working document WD 19 (992w19xx) (formerly WD 18), Grenoble, May 1999

[2] Reinhard Stolle (Infineon), *"SDSL test loops*", ETSI-TM6 temporary document TD8 (993t08a0), Edinburgh, september 1999.

[3] Dirk Daecke (Infineon), *"Scaling of SDSL testloops for different bitrates*", ETSI-TM6 temporary document TD10 (993t10a2), Edinburgh, september 1999.

[4] Jim Eyres, Consultronics, *"Wirelines and Test Loops for SDSL*", ETSI-TM6 temporary document TD18 (991t18a0), Villach, February 1999.

[5] Rob van den Brink, KPN, *Proposal for SDSL performance tests*, ETSI-TM6 contribution TD27 (984t27a0), Vienna, Sept 1998.

[6] Rob van den Brink, KPN, *Performance tests for SDSL and other long-range xDSL systems*, ETSI-TM6 permanent documents TM6(98)10, (980p10a0), Villach, Feb 1999.

[7] Letizia Tempestilli, Lorenzo Magnone (Telecom Italia Group), "*Telecom Italia proposal for inclusion of bridged taps as network impairments for SDSL feasibility study and testing purposes*". ETSI-TM6 temporary document TD28 (991t28a0) Villach, feb 1999.

[8] KPN/FSAN xDSL working group, *Self-crosstalk update of the SDSL noise models*, ETSI-TM6 contribution TD09 (992t09a0), Grenoble, May 1999.

[9] KPN/FSAN xDSL working group, *Revised noise models for SDSL*, ETSI-TM6 contribution TD20 (991t20a0), Villach, Feb 1999.

[10] Rob.F.M. van den Brink. *Cable Reference Models for Simulating Metallic Access Networks*, ETSI STC TM6 document, TM6(97)02, revision 3, June 1998.

[11] DIS 1000-4-6: *"Electromagnetic compatibility (EMC); Part4, Testing and measuring techniques; Section 6 Immunity to conducted disturbances, induced by radio frequency fields."* IEC, may 1994.

4. First estimate on loop behavior above 500kHz

Not for inclusion in the SDSL draft

	F=[0,10,20,40,100,150,200,400,500,700,1000,2000] *1000	[Hz]
"PE04"	Rs=[268,268,269,271,282,295,312,390,425,493,582,816]/1000; Ls=[680,678,675,669,650,642,635,619,608,593,582,571]/1E9; Cp=[45.5,45.5,45.5,45.5,45.5,45.5,45.5,45.5,45.5,45.5,45.5,45.5]/1E12;	Ω/m H/m F/m
"PE05"	Rs=[172,172,173,175,190,207,227,302,334,392,466,655]/1000; Ls=[680,678,675,667,646,637,629,603,592,577,572,565]/1E9; Cp=[25,25,25,25,25,25,25,25,25,25,25,25]/1E12;	Ω/m H/m F/m
"PE06"	Rs=[119,120,121,125,146,167,189,260,288,340,405,571]/1000; Ls=[700,695,693,680,655,641,633,601,590,576,570,560]/1E9; Cp=[56,56,56,56,56,56,56,56,56,56,56,56]/1E12;	Ω/m H/m F/m
"PE08"	Rs=[67,70.0,72.5,75.0,91.7,105,117,159,177.5,209,250,353]/1000; Ls=[700,700,687,665,628,609,595,568,**543+17**,553,547,540]/1E9; Cp=[37.8,37.8,37.8,37.8,37.8,37.8,37.8,37.8,37.8,37.8,37.8,37.8]/1E12;	Ω/m H/m F/m
"PVC032"	Rs=[419,419,419,419,427,453,493,679,750,877,1041,1463]/1000; Ls=[650,650,650,650,647,635,621,577,560,546,545,540]/1E9; Cp=[120,120,120,120,120,120,120,120,120,120,120,120]/1E12;	Ω/m H/m F/m
"PVC04"	Rs=[268,268,268,268,281,295,311,391,426,494,584,817]/1000; Ls=[650,650,650,650,635,627,619,592,579,566,559,550]/1E9; Cp=[120,120,120,120,120,120,120,120,120,120,120,120]/1E12;	Ω/m H/m F/m
"PVC063"	Rs=[108,108,108,111,141,173,207,319,361,427,510,720]/1000; Ls=[635,635,635,630,604,584,560,492,469,450,442,434]/1E9; Cp=[120,120,120,120,120,120,120,120,120,120,120,120]/1E12;	Ω/m H/m F/m