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SOURCE: KPN (PTT Telecom, KPN Research)
author: Rob van den Brink

CONTACT R.F.M. van den Brink
KPN Research,
PO Box 421
2260 AK Leidschendam
The Netherlands
tel: +31 70 3325389
fax: +31 70 3326477
email: R.F.M.vandenBrink@research.kpn.com

TITLE **VDSL - Proposal for VDSL testloops**

STATUS Proposal, for discussion

ABSTRACT This contribution is a proposal for the VDSL testloop topologies, as requested at the Tel Aviv meeting. The proposal includes topology, specified insertion loss for the different bitrates, expressions, line constants and plots that demonstrate the purpose and impact of the testloops. When accepted, the text can be copied literally into the VDSL draft at paragraph 10.1.

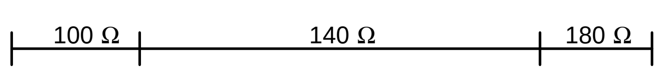
10 VDSL Performance requirements

10.1 VDSL Test loops

The purpose of the testloops in figure 1 is to stress VDSL modems in various ways, to test the VDSL performance under quasi realistic circumstances. Loop #0 is a symbolic name for a loop with zero length, to prove that VDSL can handle the signal levels when they are directly interconnected. Loop#0 is a simple representation of the shortest line that is in use in access networks.
All other testloops in figure 1 have equal insertion loss, but differ in input impedance.

- The impedances in loop 1 and 2 are nearly constant over a wide frequency interval. These two loops represent uniform distribution cables, one having a relatively low characteristic impedance and another having a relative high impedance. These impedance values are choosen to be the lowest and highest values of 0.5mm distribution cables that are *commonly* used in Europe.
- The impedances of loop 3 and 4 follow frequency curves that are oscilating in nature. This represents the mismatch effects in distribution cables caused by a short extent with a cable that differs significantly in characteristic impedance. Loop 3 represents this at the LT side to stress downstream signals only. Loop 4 does the same at the NT side to stress upstream signals only.

> ***Author suggestion****: Loop #3 represents a common Dutch situation where the underground distribution cable is extended in the central office by a commonly used indoor cable. Loop #4 represents, to our knowledge, a common British situation where the underground cable is extended by a dropwire (DW8). Loop #4 causes a severe mismatch (impedances oscillate between 100W and 250W) at the NT side that might reduce the upstream performance of VDSL modems significantly. When there is a strong demand on reducing the number of testloops, the stressing factors of loop #4 can be combined with loop #3 by extending the long 140W cable at the NT side with 180W. This mismatch is not as severe as in loop 4, but it might be a compromise to consider.*
> *The combination of* [100Ω + 140Ω + 180Ω] *lines is a reasonable compromise, that meets the requirement that both ends have a serious mismatch, similar to the LT side of loop#3 and the NT side of loop#4*



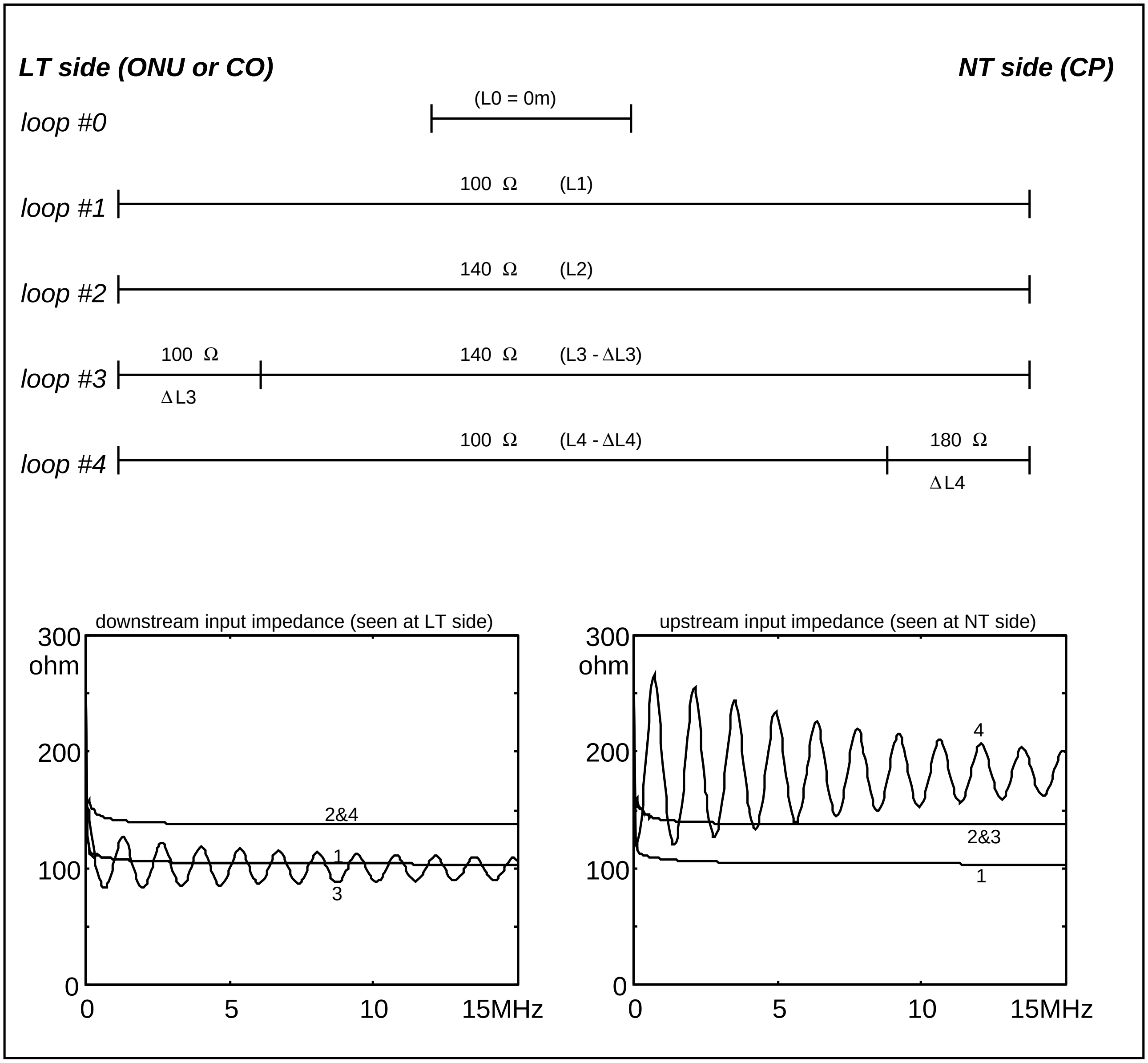


Figure 1. Test loop topology

For each VDSL bitrate, the virtual “length” of the individual testloops is defined in terms of a common insertion loss (at 135Ω), at a common frequency. This frequency is choosen to be a typical high-band frequency that is used for transporting that bitrate. The insertion loss is choosen as a typical maximum value that can be handled correctly by the VDSL modem. The higher the bitrate, the lower the insertion loss is that can be handled in practice. This is because the crosstalk in real cables increases with the frequency. Table 1 specifies these insertion loss values for the different VDSL bitrates.

> ***Author comment****: The text tries to explain in a top-down way what the purpose of the loops is, and why these loops fullfill their job. Any reference to cable diameter and physical cable length are made as low-profile as possible in this text. This to make clear that the loops are choosen because of their common use, characteristic impedance and insertion loss. The nominal length is nothing more than the result of insertion loss, not in reverse.*

VDSL bitrate	*test frequency* f_H	*insertion loss @135W, @ f_H*
6.5 Mb/s	2.5 MHz	44 dB
13 Mb/s	4 MHz	38 dB
26 Mb/s	6 MHz	28 dB
52 Mb/s	8 MHz	17 dB

Table 1. *Insertion loss for loop #1 to #4, specified for the individual bitrates.*

Author note*: At this point, we need input of VDSL manufacturers that have experience with VDSL simulations, to find out if these test frequencies are realy representative as typical high-band frequency or not. The same applies for the choosen insertion loss values. To make a good start for a proposal, we have choosen them to be equivalent with loops of nearly 1500, 1000, 600 and 300 meters.*

The different cable sections are specified by reference models [1], that serve as a template for real twisted-pair cables. The virtual lengths that meet the insertion loss requirements of table 1 are summarized in table 2. The associated modelsand line constants are specified in table 4, 5 and 6. Figure 2 shows the calculated transmission functions of the testloops, at 135Ω, to be used for the various VDSL bitrates.

test loop	*distribution cable (L)*	*extention cable (DL)* **LT or NT side**	*virtual length* D*L*	*virtual length L (6.5Mb/s)*	*virtual length L (13 Mb/s)*	*virtual length L (26 MB/s)*	*virtual length L (52 Mb/s)*
#0	--	--	--	0	0	0	0
#1	“A”	--	--	1496 m	1004 m	595 m	308 m
#2	“B”	--	--	1418 m	929 m	534 m	270 m
#3	“B”	“C”	70 m	1413 m	930 m	535 m	277 m
#4	“A”	“D”	70 m	1498 m	1002 m	585 m	292 m

Table 2. *Calculated testloop length, that meets the insertion loss requirements in table 1, based on the cable models of table 4, 5 and 6. Dit following cables models* [1] *have been used as template for these testloops: A =BT_DWUG, B =KPN_L1, C =KPN_R2 and D =BT_DW8*

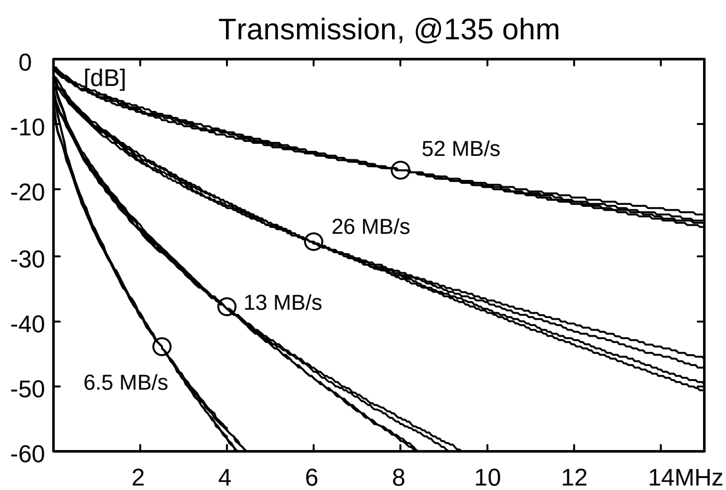


Figure 2. *Transmission (@135W) of the testloops for various bitrates, calculated using the models and line constants of table 4, 5 and 6.*

BT#0	$Z_s(f) = \sqrt[4]{R_{oc}^{4} + a_c \cdot f^2} + j \cdot 2\pi f \cdot \left(\dfrac{L_0 + L_\infty \cdot (f/f_m)^{Nb}}{1 + (f/f_m)^{Nb}}\right)$	[Ω/km]
	$Y_p(f) = (g_0 \cdot f^{Nge}) + j \cdot 2\pi f \cdot (C_\infty + C_0 / f^{Nce})$	[S/km]
	$Z_{s0}(\omega) = j \cdot \omega \cdot Z_{0\infty} \cdot 1/c + R_{ss00} \cdot (1 + K_l \cdot K_f \cdot (\chi \cdot \coth(4/3 \cdot \chi) - 3/4))$	[Ω/m]
KPN#1	$Y_{p0}(\omega) = j \cdot \omega / Z_{0\infty} \cdot 1/c \cdot (1 + (K_c - 1) / (1 + (\omega/\omega_{c0})^N)) + \tan(\phi)/(Z_{0\infty} \cdot c) \cdot \omega^M$	[S/m]
	$\chi = \chi(\omega) = (1+j) \cdot \sqrt{\dfrac{\omega}{2\pi} \cdot \dfrac{\mu_0}{R_{ss00}} \cdot \dfrac{1}{K_n \cdot K_f}}, \quad \omega_{c0} = 2\pi \cdot f_{c0}$	

Table 4. *Formal models for the BT and the KPN cable parameters in the testloops*

Wire type	R_{oc} N_b	a_c g_0	R_{os} N_{ge}	a_s C_o	L_o **C¥**	**L¥** N_{ce}	f_m
A	179 1.2	35.89e-3 0.5e-9	0.0 1.033	0.0 1e-9	0.695e-3 55e-9	585e-6 0.1	1e6
D	41.16 1.1952665	1.2179771e-3 53.0e-9	0.0 0.88	0.0 31.778569e-9	1e-3 22.681213e-9	910.505e-6 0.11086674	174877.

Table 5. *Line constants for the BT cables in the testloops. The models are valid from DC to 30 MHz, when using these parameters.*

	$Z_{0\infty}$	c/c_0	R_{ss00}	$2\pi \tan(\phi)$	K_f	K_l	K_n	K_c	N	f_{c0}	M
B	136.651	0.79766	0.168145	0.13115	0.72	1.2	1	1.08258	0.7	4521710	1
C	97.4969	0.639405	0.177728	0.0189898	0.5	1.14	1	1	1	100000	1

Table 6. *Line constants for the KPN cables in the testloops. The models are valid from DC to 30 MHz, when using these parameters.*

***Author note**: We should NOT start a political discussion on which cable model is the best of these two, just to save 4cm of text in the VDSL report. There are more models in use* [1] *, and these models are OK when they do their job right. We are specifying loops here, not models, and the full two-port behaviour of the testloop cables should be defined from DC up to some upper frequency, say 30MHz. Models are no more than a vehicle to achieve this. So, when we agree on a cable for which an adequate model is available, then we should use that model.*

References

[1] Rob van den Brink: **Cable reference models for simulating metallic access networks ,** ETSI-TM6 permanent document ETSI/STC TM6(97)02, [970p02r1], Berlin, Germany, 2-8 june 1997.