TITLE **Modified insertion loss specs for the VDSL testloops**

PROJECT VDSL

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STATUS Proposal, for action

ABSTRACT In the Lannion meeting, the payload bitrates have been changed, so the insertion loss specification of the testloops must change accordingly. This contribution proposes modified specifications for the testloops: one for each bitrate combination.

Problem description

In the Lannion meeting, the payload bitrates have changed. It is possible that these bitrates will change again or that new bitrates will be added. This contribution proposes consistent testloop specifications for these (and future) bitrates, and a systematic approach to find them for arbitrary bitrates.
The specified insertion loss, specified at a dedicated test frequency, is calculated from the results of two simple (empirical) expressions. One maps the bitrate into a target test frequency, and another into a target length for testloop #1. The resulting values that are proposed here, is in line with the performance that ETSI-TM6 has expected for a long time. Nevertheless, it is possible that some of the resulting test frequencies are not considered as representative, or that some of the insertion loss specifications is not considered as realistic. In that case, amendments to this proposal should focus on the two empirical expressions that have been used. All the rest is a simple matter of straight forward mathematics.

The proposed text below, can be copied literally into the VDSL draft, when accepted. It is restricted to the missing parts, the parts that should be updated, or that should change in order.

9. Transmission performance

9.1 Test loops

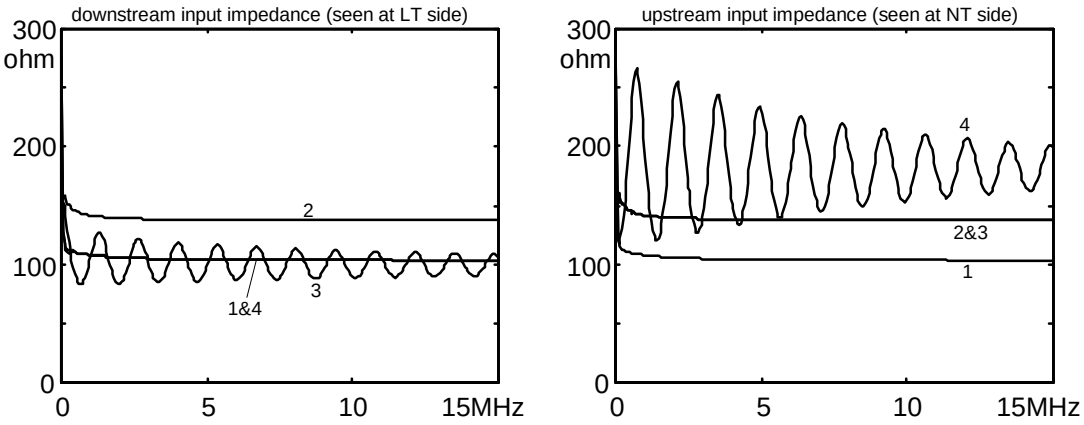

Figure 12. *Calculated variation of input impedance, at a length of 1500m.*

VDSL payload code		Downstream payload bitrate	Upstream payload bitrate	Test frequency f_T	Insertion loss @135W, @ f_T
A1	(6N/2N)	6 × 1.024Mb/s	2 × 1.024Mb/s	2.5 MHz	47 dB
A2	(12N/2N)	12 × 1.024Mb/s	2 × 1.024Mb/s	4.0 MHz	37 dB
A3	(24N/4N)	24 × 1.024Mb/s	4 × 1.024Mb/s	6.0 MHz	25 dB
S1	(6N/6N)	6 × 1.024Mb/s	6 × 1.024Mb/s	3.5 MHz	39 dB
S2	(12N/12N)	12 × 1.024Mb/s	12 × 1.024Mb/s	5.5 MHz	27 dB
S3	(24N/24N)	24 × 1.024Mb/s	24 × 1.024Mb/s	8.0 MHz	18 dB
S4	(36N/36N)	36 × 1.024Mb/s	36 × 1.024Mb/s	9.0 MHz	14 dB

Table 3. *Insertion loss and test frequencies (f_T) for loops #1 to #4, for various payload bitrates.*

The magnitude of the testloop insertion loss shall approximate the insertion loss of the specified models within 3% on a dB scale, between $0.1 \times f_T$ and $3 \times f_T$. The phase of the testloop insertion loss may deviate from the specified models. This enables a length adjustment to meet these insertion loss magnitude requirements with real cables.
The magnitude of the testloop characteristic impedance shall approximate the characteristic impedance of the specified models within 7% on a linear scale, between $f_T/3$ and $f_T \times 3$.

Test loop	Distribution cable (L)	Extention cable (DL) LT or NT side	Extention length DL
#0	--	--	--
#1	"A"	--	--
#2	"B"	--	--
#3	"B"	"C"	70 m
#4	"A"	"D"	70 m

Table 4. *Testloop composition. The labels "A" to "D" refer to the cable models, summarized in Annex A:*
"A"=BT_dwug, "B"=KPN_L1, "C"=KPN_R2, "D"=BT_dw8.

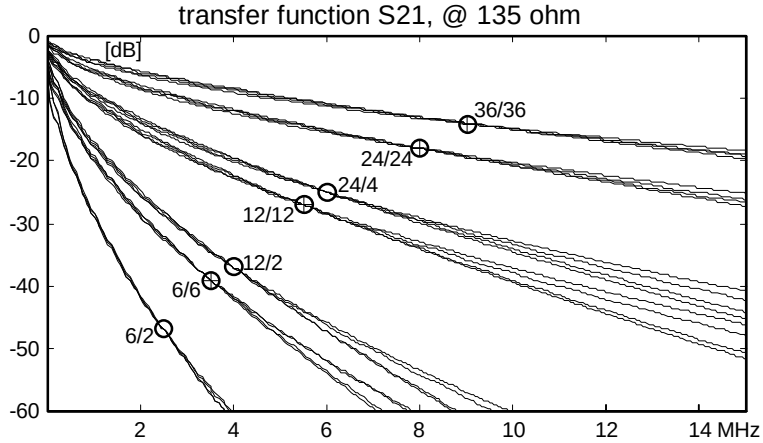

Figure 18. *Transmission (in 135W) of the testloops for various payload bitrates*

Annex A [normative]
Primary line constants for the test loop-set

Test loop	length L (6N/2N)	length L (12N/2N)	length L (24N/4N)	length L (6N/6N)	length L (12N/12N)	length L (24N/24N)	length L (36N/36N)
#0	0	0	0	0	0	0	0
#1	1598 m	978 m	531 m	1107 m	601 m	327 m	238 m
#2	1514 m	904 m	477 m	1032 m	544 m	286 m	207 m
#3	1510 m	905 m	478 m	1027 m	547 m	293 m	213 m
#4	1600 m	976 m	520 m	1099 m	595 m	310 m	219 m
avg	***1556 m***	***941 m***	***501 m***	***1066 m***	***572 m***	***304 m***	***219 m***

Table x. *Calculated length of the testloops various bitrates. These lengths are calculated with the models and line constants of table 10 and 11. The actual lengths may deviate from this because real testloops have to meet the insertion loss requirements in stead of lenght requirements*

Rationals behind the various insertion loss specifications
Each bitrate is stressed by a dedicated insertion loss value, specified at a dedicated test frequency f_T. Their choice for a downstream bitrate of x·N and an upstream bitrate of y·N (N=1.024 Mb/s) is directly related to the value (x+y). The specified values are selected according to the following patterns:

- The test frequency is assumed to be a highband representative for the frequency spectra that will be generated for these bitrates. The chosen value of f_T is the rounded value of a target value that equals: $(f_{TT} / 10^6) = 7\times {}^{10}\log(x+y) - 4$.
- The insertion loss at test frequency f_T is a rounded value, that causes a length for testloop #1 that approximates a special target length. That length equals" $(L_T/1000)= 9.7\times10$.^$(-0.87\times{}^{10}\log(x+y))$.

This approach makes the testloops consistent for the different bitrates.