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TITLE

Proposal for overview of concepts in Annex X: Solid-state quantum computing.

PROJECT FGQT Roadmap
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ABSTRACT

In this contribution we provide a start for an overview of the concepts used in “Annex X: Solid-state Quantum Computing“. (see N058a). For the time being we refer to it as annex „X“, but that should be replaced by the appropriated number when the Roadmap Editor has updated the draft. This proposal builds on “Proposal for terminology in Annex X: Solid-state quantum computing.”

Explanation of changes

Provide a first proposal for an overview of concepts.

Why are the changes needed?

There is no content yet.

1 **X.3 Overview of concepts**

2 *A quantum schedule* describes when which operation should be applied on what. At the gate
 3 level, the quantum schedule is equivalent to a circuit diagram. A circuit diagram specifies the
 4 order in which gates and measurements are applied to qubits. At the pulse level, the quantum
 5 schedule is equivalent to a pulse diagram. A pulse diagram specifies at what time, which
 6 pulses are applied to which location on a quantum device (a port) and at which frequency (a
 7 clock). The hardware-instruction level description specifies when which instructions need to
 8 be executed in the control electronics in order to generate the desired pulses at the quantum
 9 device. The hardware-instruction level description is implementation-specific.

10 Table 1 gives an overview of these different layers.

Table 1 Overview of concepts and their representation at different levels of abstraction.

	Abstraction layer	Quantum-circuit level	Quantum-device level
	Describes	Gates acting on ideal qubits	Signals on a quantum device
When	Schedule	Order of operations	Timing of operations
What	Operation	unitaries and POVMs	parameterized waveforms and acquisition protocols
Where	Resource	qubits	ports & clocks

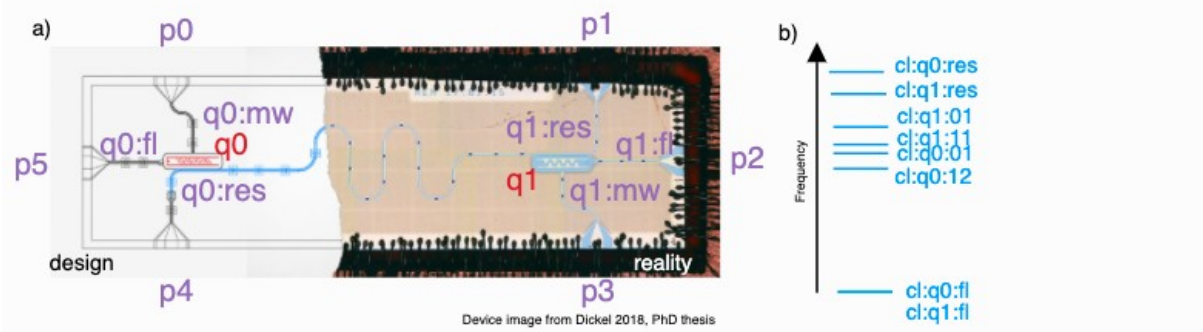
11 **Example: resources on a transmon device**

12 Resources denote where an operation should be applied. Here we explain these concepts using
 13 a simple cQED device shown in Fig. 2. These concepts should be easy to generalize to other
 14 devices and systems.

15 For many systems, it is possible to associate a qubit with an element or location on a device
 16 that a signal can be applied to. We call such a location on a device a port. Here, qubits and
 17 ports are represented as strings (e.g., `P0`, `feedline_in`, `q0:mw_drive`, etc.). A port can be
 18 associated with a qubit by including the qubit name in the name of the port (separated by a
 19 colon `:`).

20 Besides the physical location on a device, a pulse is typically applied at a certain frequency. A
 21 reference clock can be used to track the phase of a certain transition or simply to ensure the
 22 signal ends up at the right frequency. Similar to ports, reference clocks can be associated with
 23 qubits by including it in the name, but this is not required to account for non-qubit elements.

1 If the frequency of a clock is set to 0 (zero), the pulse is applied at baseband and is assumed to
 2 be real-valued.



3
 4 *Fig. 2 Resources are used to indicate on what operations are applied. (a) Ports (purple)*
 5 *indicate a location on a device. By prefixing the name of a qubit in a port name (separated by*
 6 *a colon `:`) a port can be associated with a qubit (red), but this is not required. (b) Clocks*
 7 *(blue) denote the location in frequency space and can be set to track the phase of a known*
 8 *transition. By prefixing the name of a qubit in a clock name (separated by a colon `:`) a clock*
 9 *can be associated with a qubit (red), but this is not required. Device image from [Dickel](#)*
 10 *(2018) .*

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