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TITLE Dedicated text for describing photonic architectures

PROJECT FGQT Roadmap

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SOURCE Ben Kassenberg (QuiX, The Netherlands) b.kassenberg@quix.nl
Pim Venderbosch (QuiX, The Netherlands), p.venderbosch@quix.nl
Rob F.M. van den Brink (Delft Circuits, The Netherlands),
Rob.vandenBrink@Delft-Circuits.com
Wouter Vlothuizen (TNO, The Netherlands), wouter.vlothuizen@tno.nl
Niels Bultink (QBLOX, The Netherlands), niels@qblox.nl
Peter Verhoeff (TNO / Quantum Inspire), peter.verhoeff@tno.nl

ABSTRACT

Explanation of changes

We propose an extension to the existing section 4.3 (quantum computing) as well as adding a dedicated annex, to cover technology for photonic quantum computers as well.

Why are the changes needed?

To handle the complexity of quantum computing as-a-whole, it is essential to subdivide these systems into much smaller modules in order to set requirements about them.

So far, the present section 4.3.4 of the Roadmap Document describes the modularity and layering of the hardware stack for only “solid-state based quantum computing” and leaves other architecture solutions for further study.

This contribution proposes such modularity for a complementary solution, and we have called that architecture “photonic based quantum computing”.

1. Situation sketch

Standardisation is about setting requirements on devices / units / modules / layers of a system such that products from different suppliers can have well-defined interfaces and can interwork with other products into a well-functioning system. The modularity to-be-defined is only usable for standardisation when clear interfaces can be identified between them such that they can be offered by different suppliers/vendors.

Section 4.3.4 elaborates on the modularity and layering of the hardware stack, and this has only been defined for an architecture group that we have called “solid-state based quantum computing”. And since this alone covers already quite a lot of technologies / implementations, it has been elaborated in further detail in a dedicated annex (E).

In this contribution, we propose a similar approach for a second architecture group, which we have called “photonic based quantum computing”. These architectures are complementary to the first one, are complex as well, and deserve a dedicated annex too. That annex may also grow into a future standard(s).

This contribution proposes two text blocks. The first block is for “announcing” this second architecture in section 4.3.4, and the second block is to make a start with content for a dedicated annex (annex F for the time-being). In order to integrate nicely with existing text, we propose to replace the current text in 4.3.4 by the full text below. Note that “NV Centers” have moved from section 4.3.4.1 to 4.3.4.3.

Proposal for updating introduction of section 4.3.4

4.3.4. Modularity and layering of hardware stack

Quantum computing is an area covering very different architectures and each architecture has its own dedicated implementation. A convenient way of describing them is by using a layered stack, ranging from hardware at the bottom to software at the top.

When needed, each layer can be subdivided into different modules that are dedicated to a specific architecture.

Figure 4.1 illustrates a subset of such layering and modularity, currently dedicated to two complementary architectures. One for “solid-state based quantum computers” and another one for “photonic based quantum computers”. Table 1 offers suitable names for these modules. Since these two do not cover all possible solutions, the missing ones are represented by “other solutions” until dedicated descriptions are proposed.

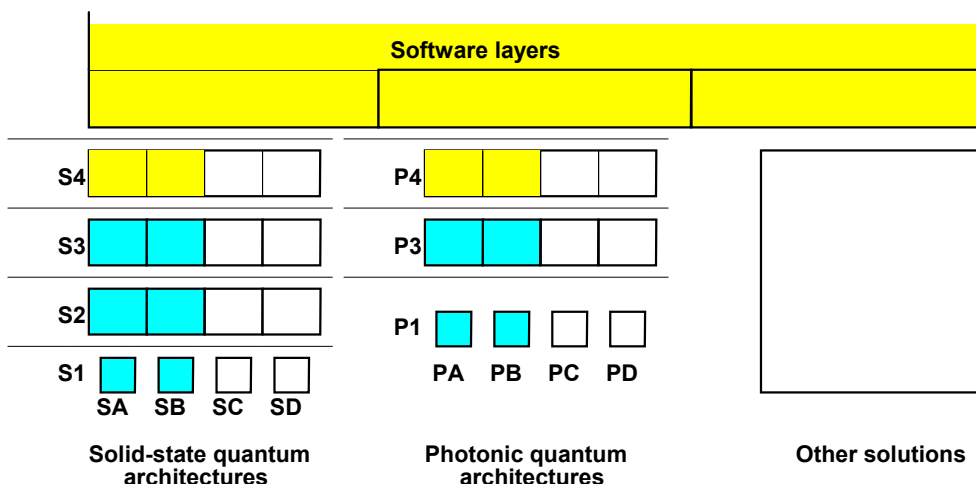


Figure 1. A first break-down of quantum computing architectures into various modules

Solid-state based quantum architectures	Photonic based quantum architectures	Other architectures
S1 = Quantum device S2 = Quantum control highway S3 = Quantum control electronics S4 = Quantum control software	P1 = Quantum photonic devices P3 = Quantum control Electronics P4 = Quantum control software	Layers for other solutions
Sa = Transmons Sb = Spin Qubits Sc = (some future development) Sd = (some other future development)	Pa = Boson sampling Pb = Gate based quantum computing Pc = (some future development) Pd = (some other future development)	Implementations for other solutions

Table 4.1. Naming of the various modules in figure 4.1.

Further details about this layering have been described below.

4.3.4.1 Solid-state based quantum computing architecture

These architectures have in common that they all make use of a cryogenic fridge, where the quantum device is controlled from outside the fridge by room-temperature electronics. Consequently, a huge amount of control channels is required to interconnect those two, especially when many qubits are to be controlled in a single fridge.

The following layers have been identified:

- *Quantum devices* - The devices in layer S1 are typically operating at cryogenic temperatures, and may be implemented as chip and/or on PCB.
- *Control highway* - Layer S2 covers all infrastructure needed for transporting microwave, RF and DC signals (via electrical and/or optical means) between the control electronics at room temperature and the quantum device at cryogenic temperatures. It is a mix of transmission lines, filtering, attenuation, amplification, (de)multiplexing, etc. A huge number of control channels are required to control many qubits in a single fridge (which clarifies the name) and this can easily become very bulky. It has also tough requirements on aspects like heat-flow, thermal noise and vacuum properties.
- *Control electronics* - Layer S3 covers all electronics for generating, receiving, and processing microwave, RF and DC signals. Some implementations make use of routing/switching and/or multiplexing of control signals at room temperatures.
- *Control software* - Layer S4 covers all low-level driver software and other low-level software for instructing the control electronics what signals should be generated or detected, and at what control channel. It also has a software interface to receive instructions about what pulses are to be generated, how to read-out the response of each and how to perform calibration.

Further details about solid-state based quantum computing have been elaborated in annex E

4.3.4.2 Photonic-based quantum computing

These architectures have in common that they rely on optical principles. The following layers have been identified:

- *Quantum photonic devices* - Layer P1 contains sources, detectors, (non)linear optical devices, and feedback mechanisms. These devices are combined into a quantum photonic architecture. Note that all wiring is included in this layer, and that a dedicated layer "P2" has not been defined.
- *Control Electronics* - Layer P3 contains all electronics to control and read-out the quantum devices in the layer below.

- Control software – Layer P4 covers all low-level driver software for instructing signal generation and processing.

Further details about photonic-based quantum computing have been elaborated in annex G

4.3.4.3 Atom based quantum computing

These architectures have (artificial) atom based qubits. For instance NV centers and Ion-traps.

EDITORIAL NOTE: Some further study is required to define this category of architectures, so that a separate contribution can be made.

Editorial note: There are more architectures on quantum computing, each with a different state of maturity. Experts, who are more dedicated to those architectures are invited to elaborate on relevant text and naming for this section

End of literal text proposal in 4.3.4

Proposal for adding a dedicated annex G(?)

Annex G. Photonic Quantum Computing

G.1 Scope and objectives

The aim of this annex is to break-down the hardware stack of quantum computers based on photonic architectures into smaller layers and modules. The functionality of each of the identified modules must be identified in such a manner that they can interwork with each other via well-defined interfaces. This annex is also the natural place to collect what kind of requirements on these modules deserve a specification in future standards. The specification of actual values is beyond the scope of this present annex.

As such, the structure identified in this annex could grow into a (future) dedicated standard on photonic quantum computing.

G.2 Terminology

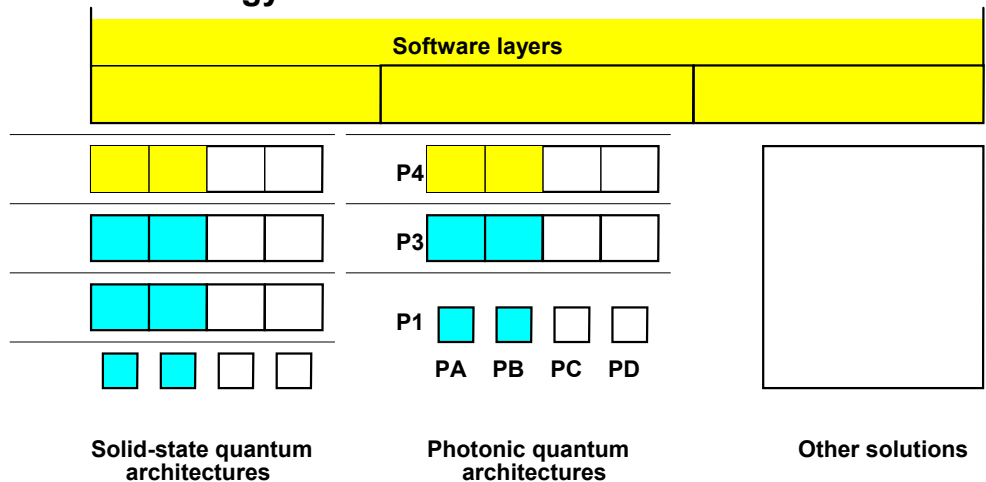


Figure G.1. A possible break-down into various modules for photonic quantum computing architectures

Layers	Architectures
P1 = Quantum photonic devices P3 = Quantum control Electronics P4 = Quantum control Software	Pa = Boson sampling Pb = Gate based quantum computing Pc = (some future development) Pd = (some other future development)

Table G.1. Naming of the various modules in figure G.1

G.3 References

Editorial note: This paragraph is intended for referencing to other standards (if any)

G.4 Quantum photonic devices

This section contains all quantum photonic devices that are necessary for a photonic quantum computing architecture. This includes sources, detectors, (non)linear optical devices, and feedback mechanisms. These elements can be combined in various ways to create different types of photonic quantum computers. For example a boson sampler (implementation Pa) needs a set of photon sources, a photonic processor (linear optical device) and a set of photon detectors.

The different devices are shown in fig. G.2 where the devices are split up into minimally required devices and additional devices. The minimally required devices for a photonic quantum computer are sources, detectors, and linear optics. The additional devices are nonlinear optics and feedback. They add functionality and allow for different computing protocols to be used and therefore allows different applications to be run.

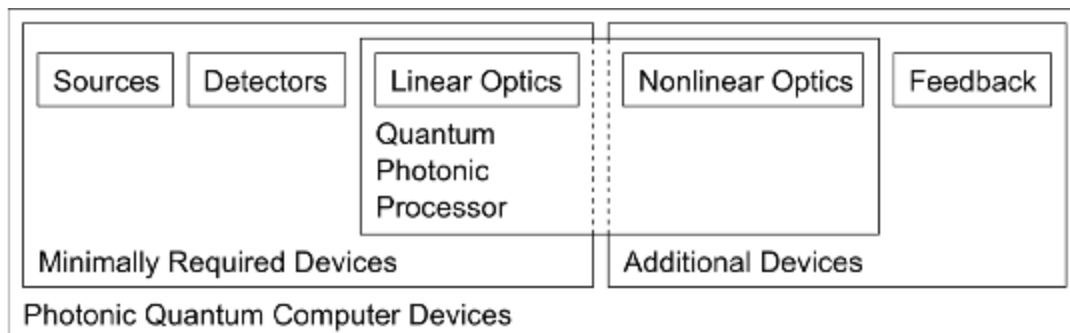


Figure G.2. A diagram of the photonic quantum computer devices organized into several categories. The devices are split up into minimally required devices and additional devices, where sources, detectors and linear optics belong to the former category, and nonlinear optics and feedback to the latter. A quantum photonic processor consists of linear optical devices, but it can also include nonlinear optical devices.

Examples of various elements are listed below together with their requirements:

G.4.1 Photonic Sources

- Examples
 - Spontaneous Parametric Down-Conversion (SPDC)
 - Quantum Dot
 - Ring Resonator

- etc.
- Requirements
 - Generation rate (number of photons per second)
 - Wavelength (center wavelength of the photon's spectrum)
 - Spectrum (wavelength distribution of the photons)
 - Repetition rate of pump laser
 - Efficiency (probability of generating a single photon (pair) per pump pulse)
 - Distinguishability (wavefunction overlap integral of the photons)

G.4.2 Photonic Detectors

- Examples
 - Avalanche Photo Diode (APD)
 - Superconducting Nanowire Single Photon Detector (SNSPD)
 - Photon Number Resolving Detector
 - etc.
- Requirements
 - Efficiency as a function wavelength (probability that a photon with a specific center wavelength is detected)
 - Dark counts (number of detections per second without incoming photons)
 - Jitter (timing inaccuracy)
 - Dead time (time that detectors are insensitive to incoming photons after a detection event)
 - Pulse shape (temporal shape of the electrical signal generated by the detectors)

G.4.3. Linear Optics

- Examples
 - waveguides
 - directional couplers
 - ring resonators
 - tunable beam splitters
 - phase shifters
 - etc.
- Requirements
 - Loss
 - Fidelity, measure of accuracy for operation implementation
 - Tunability, degree of control over the operations
 - Dispersion
 - Number of input and output modes (physical waveguides)
 - Circuit depth, number layers of optical elements

G4.4. Nonlinear Optics

- Examples
 - Quantum Dot
 - Doped waveguide (gain region)
 - etc.
- Requirements
 - Loss

- Gain
- Efficiency
- etc.

G.4.5 Feedback

- Examples
 - -
- Requirements
 - -

G.5 Quantum Control Electronics

This section contains all electronics that is needed to control the quantum devices in lower layers. And the connections to a PC so that the control signals can be sent to the control electronics.

- Examples
 - TEC + PID
 - Drivers for tuneable elements on photonic processor
 - (micro)processor for drivers and TEC
 - Time tagger for detector signals
 - (Bias current source for detectors)
 - Connection hardware (USB/COM)
- Requirements:
 - <to be identified>

G.6 Quantum Control Software

This layer contains the low-level driver software that is needed to drive the control hardware and communicate with higher software layers.

Covers:

- Software driver

Requirements:

- Connection protocol (for instance serial or API)
- Speed
- Features

End of literal text proposal in Annex G
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